IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

EMC CORPORATION, EMC INTERNATIONAL COMPANY, and EMC INFORMATION SYSTEMS INTERNATIONAL, Plaintiffs, v. PURE STORAGE, INC., Defendant.	Civil Action No. 13-1985

MEMORANDUM OPINION

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ANDREWS, U.S. DISTRICT JUDGE:

Before this Court is the issue of claim construction of disputed terms found in five U.S. Patents, 6,904,556 ("the '556 patent"), 6,915,475 ("the '475 patent"), 7,373,464 ("the '464 patent"), 7,434,015 ("the '015 patent"), and 8,375,187 ("the '187 patent").

I. BACKGROUND

Plaintiffs assert that Defendant infringes several of their patents in the field of data storage systems. (D.I. 92 at p. 3). The Court has considered the parties' claim construction briefing (D.I. 92, 93, 95) and held a Markman hearing on December 16, 2014.[1]

II. LEGAL STANDARD

"It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal quotation marks omitted). "'[T]here is no magic formula or catechism for conducting claim construction.' Instead, the court is free to attach the appropriate weight to appropriate sources 'in light of the statutes and policies that inform patent law.'" *SoftView LLC v. Apple Inc.*, 2013 WL 4758195, at *1 (D. Del. Sept. 4, 2013) (quoting *Phillips*, 415 F.3d at 1324). When construing patent claims, a matter of law, a court considers the literal language of the claim, the patent specification, and the prosecution history. *Markman v.*

[1] Per an order of this Court, the parties were limited to ten terms for argument at the hearing. They argued: "determine" / "determined" / "determining"; "probabilistic summary"; "identifier(s)"; "return" / "returning"; "scheduled"; "any available address location"; "block(s) of data"; "associated with the transmitted blocks of data"; "memory board"; and "memory region." (D.I. 95 at p. 2). This Memorandum Opinion, however, will construe all eighteen terms submitted by the parties in the briefing.

Westview Instruments, Inc., 52 F.3d 967, 977–80 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). Of these sources, "the specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315 (internal quotation marks and citations omitted).

"[T]he words of a claim are generally given their ordinary and customary meaning. . . . [Which is] the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1312–13 (internal quotation marks and citations omitted). "[T]he ordinary meaning of a claim term is its meaning to [an] ordinary artisan after reading the entire patent." *Id.* at 1321 (internal quotation marks omitted). "In some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." *Id.* at 1314 (internal citations omitted).

A court may consider extrinsic evidence, which "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises," in order to assist the court in understanding the underlying technology, the meaning of terms to one skilled in the art, and how the invention works. *Id.* at 1317–19 (internal quotation marks and citations omitted). Extrinsic evidence, however, is less reliable and less useful in claim construction than the patent and its prosecution history. *Id.*

"A claim construction is persuasive, not because it follows a certain rule, but because it defines terms in the context of the whole patent." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). It follows that "a claim interpretation that would

exclude the inventor's device is rarely the correct interpretation." *Osram GmbH v. Int'l Trade Comm'n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007) (internal quotation marks and citation omitted).

III. CONSTRUCTION OF DISPUTED TERMS

A. The '464 and '015 Patents

Claim 1 of the '464 patent is representative:

> A method for storing data comprising:
>
> receiving a data stream comprising a plurality of data segments wherein each data segment is associated with an *identifier*;
>
> *determining* using a subset of *identifiers* that are stored in a low latency memory whether a data segment has been previously stored; and
>
> *returning* the *identifier* for the data segment in the event the data segment is *determined* to have been stored previously.

('464 patent, claim 1).[2]

Claim 1 of the '015 patent is representative:

> A method for storing data comprising:
>
> receiving a data stream comprising a plurality of data segments;
>
> assigning an *identifier* to one of the plurality of data segments; and
>
> *determining* whether one of the plurality of data segments has been stored previously using a summary, wherein the summary is a space efficient, *probabilistic summary* of segment information.

('015 patent, claim 1).

1. "determine" / "determined" / "determining" ('464 patent – claims 1, 19, 32; '015 patent – claims 1, 15, 16).

[2] The patent actually says, "a data segments," but the parties agree that that is a recurring typo, and should be read as "a data segment" wherever the phrase appears.

a. *Plaintiffs' proposed construction*: Decide/decided/deciding, either conclusively or inconclusively.

b. *Defendant's proposed construction*: Conclusively decide/decided/deciding.

c. *Court's construction*: Decide/decided/deciding, either conclusively or inconclusively.

The Court agrees with Plaintiffs that "determine" must be construed as being decided either conclusively or inconclusively. Both patent specifications explicitly refer to positive, or conclusive determinations, implying that a determination can be either conclusive or inconclusive. *See, e.g.,* '464 patent at 5:46-67 ("The cache can positively (that is, conclusively) determine that the segment ... has previously been stored, because it is found in the cache." *Id.* at 5:46-49). At the hearing, both parties agreed that positive and positively mean conclusive and conclusively. (D.I. 108 at 25-26). The patent claims also support the idea that determining can be either conclusive or inconclusive. Dependent claim 2, for example, provides that "the determination [from claim 1] can positively confirm that the data segment has been previously stored, but cannot positively confirm that the data segment has not been previously stored." ('464 patent at 10:15-18). In response to this, Defendant has asserted that the specification "emphasizes" conclusive determinations and that the specification does not disclose any examples of inconclusive determinations. (D.I. 92 at p. 12). Instead, according to Defendant, the specification "only discloses situations where no determination can be made." (*Id.*). Even if true that the specification only discloses or emphasizes conclusive determinations, the specification and claims demonstrate that determinations are qualified with "positively" when decided conclusively. A determination that is not "positive," therefore, must have some independent meaning—a determination cannot be conclusive both when it is, and is not,

described as "positive." Therefore, the Court construes "determine" as "decide either conclusively or inconclusively."

2. "probabilistic summary" ('015 patent – claims 1, 15, 16).

a. *Plaintiffs' proposed construction*: A data structure that indicates, with possible uncertainty, whether a data segment is already stored.

b. *Defendant's proposed construction*: low latency memory subsystem (such as a Bloom filter), that can conclusively determine that a received data segment has not already been stored.

c. *Court's construction*: A data structure that indicates, with possible uncertainty, whether a data segment is already stored.

Defendant asserts that because the specification states that probabilistic summary "can positively determine that the segment has not been stored," it should be construed as "conclusively determin[ing]." (D.I. 92 at p. 19; *see, e.g.,* '015 patent at 5:44-45). Dependent claim 6, however, recites that "the determination [from the probabilistic summary] can positively determine that one of the plurality of data segments has not been stored previously, but cannot positively determine that the one of the plurality of data segments has been stored previously." ('015 patent at 10:5-9). For similar reasons to above, because the patent claims contemplate both conclusive and inconclusive determinations, even if the specification did not provide examples of inconclusive determinations, the claims should be construed as allowing them.

It is also a bad idea to import the reference to the Bloom filter into the construction. The specification explains that "[i]n one embodiment, the summary is implemented using a summary vector," and that one example of such a summary vector is a Bloom filter. ('015 patent at 8:56-

58). The Bloom filter is clearly stated to be exemplary, implying that there can be, and are, other examples of summary vectors. The patent, in dependent claim 14, limits "summary" to a Bloom filter. *See* '015 patent at 10:55-56 ("A method for storing data as recited in claim 1 wherein the summary is a Bloom filter."). There is no reason to construe probabilistic summary in such a way as to suggest that it is a Bloom filter.

Therefore, the Plaintiffs' construction is adopted.

3. "identifier(s)" ('464 patent - claims 1, 3, 5, 13, 19, 21, 32; '015 patent - claims 1, 2, 4, 13, 15, 16).

a. *Plaintiffs' proposed construction*: Plain and ordinary meaning.

b. *Defendant's proposed construction*: unique value for an individual data segment.

c. *Court's construction*: Information that identifies a data segment.

At the hearing, Plaintiffs explained that the plain and ordinary meaning of identifier is "information that identifies a data segment." (D.I. 108 at 52-53). The Court agrees. At the hearing, Defendant agreed that it was fine with "information," stressing, however, that the identifier(s) must be unique. (D.I. 108 at 55-56). The patents refer to "short identifiers," which, according to the specification, "are not likely to be unique." ('464 patent at 6:10). Dependent claim 13 refers to the short identifier. *See, e.g.,* '014 patent at 10:49-52. According to Defendant, this should not matter because short identifiers are not "identifiers." (D.I. 92 at p.

24). The Court disagrees. Short identifiers must be "identifiers." Therefore, identifiers do not necessarily have to be unique, and the Plaintiffs' construction is correct.[3]

4. "return" / "returning" ('464 patent - claims 1, 19, 32).

a. *Plaintiffs' proposed construction*: Plain and ordinary meaning.

b. *Defendant's proposed construction*: deliver back to the calling routine / delivering back to the calling routine.

c. *Court's construction*: deliver back / delivering back.

The Court is inclined to use the plain and ordinary meaning of "return," but at the hearing, Plaintiffs argued that that meaning would be deliver, implying that there does not have to be a return to a point of origin. (D.I. 108 at 60-61). The Court disagrees. The plain and ordinary meaning of return is deliver back. In the briefing, Defendant sensibly agreed not to limit the term to software implementations as it may encompass non-software ones, such as a "delivering module." (D.I. 92 at p. 29). The Court agrees. The explicit limitations proposed by Defendant, however, "to the calling routine or delivering module" may nonetheless incorrectly limit the construction. Therefore, the plain and ordinary meaning, deliver back, must control.

B. The '187 Patent

Claim 1 of the '187 patent is representative:

> Apparatus for controlling the scheduling of data transfers between a *buffer memory* and a plurality of solid state storage devices in a data storage system, the apparatus comprising:

[3] In subsequent terms, when the Court adopts the "plain and ordinary meaning," it is necessarily rejecting the Defendant's proposed limitations. *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1361-62 (Fed. Cir. 2008).

a controller for designating at least one of the plurality of solid state storage devices as a current write device such that there is always at least one solid state storage device *scheduled* as a current write device;

the controller designating the remainder of the plurality of solid state storage devices as current read device(s);

the controller storing write data from a host in the *buffer memory*;

the controller allowing storage device reads to occur only from the current read device(s);

the controller allowing storage device writes to occur only to the current write device(s) and to *any available address location* of the current write device(s);

the controller, responsive to *a* triggering event, updating the designations to cause a different and at least one of the plurality of solid state storage devices to be designated a new current write device, and the remainder of the plurality of solid state storage devices to be designated the current read device(s), wherein, as prerequisite to accomplishing the update of the designations, the controller allows *write operations pending* for each current write device to finish to that current write device and reads to occur from any of the solid state storage devices, including from each current write device.

('187 patent, claim 1).

1. "a" in the phrase "a triggering event" ('187 patent - claims 1, 5, 9, 12).

    a. *Plaintiffs' proposed construction*: One or more

    b. *Defendant's proposed construction*: Construction is not necessary

    c. *Court's construction*: One or more.

In patents, "a" is usually construed to be "one or more." Defendant argues that no construction is necessary because "'a' in the phrase 'a triggering event' means one and only one triggering event." (D.I. 92 at p. 31) (citations omitted). The Court disagrees that construction is not necessary. The specification, for example, explains that a triggering event "may include but not be limited to" nine examples, then stating as the tenth example, "any combination of the

above." *See* '187 patent at 6:26-46. If a triggering event could be one event, or any combination of multiple triggering events, "a" must (as it usually does) mean one or more. Therefore, Plaintiffs' construction is adopted.

2. "buffer memory" ('187 patent - claims 1, 5, 9, 12).

a. *Plaintiffs' proposed construction*: Memory for temporary storage of data

b. *Defendant's proposed construction*: cache in global memory for temporary data retention.

c. *Court's construction*: Memory for temporary storage of data

The Court agrees with Plaintiffs that Defendant is improperly equating buffer memory with cache. (D.I. 92 at p. 34). The patent appears to contemplate different types of buffer memory, and cache is but one example. ('187 patent at 5:14-16). The patent also references a system where global memory "includes (among other things)" a cache memory, but that is "an illustrative example," according to the patent, implying that other examples without these limitations are possible. ('187 patent at 3:31-42). Therefore, Plaintiffs' proposed construction is adopted.

3. "scheduled" ('187 patent - claims 1, 5, 9, 12).

a. *Plaintiffs' proposed construction*: Plain and ordinary meaning

b. *Defendant's proposed construction*: currently selected by the controller in accordance with a scheduling policy

c. *Court's construction*: Plain and ordinary meaning.

At the hearing, Plaintiffs explained that the plain and ordinary meaning of "scheduled" is "designated," and this Court agrees. (D.I. 108 at 73-74). Claims 1 and 9 already expressly reference a controller. *See, e.g.*, '187 patent at 12:40-43 ("...the controller allows write operations pending for each current write device to finish to that current write device..."). Therefore, the Court finds reference to that phrasing to be redundant in a construction. The Court also does not find any support for the inclusion of "currently" in the construction, especially because "current" appears throughout the claims where the patentee wanted to indicate a particular timing. *See, e.g.*, '187 patent, claim 1. Therefore, the Court adopts Plaintiffs' construction.

4. "any available address location" ('187 patent - claims 1, 5, 9, 12).

a. *Plaintiffs' proposed construction*: Plain and ordinary meaning.

b. *Defendant's proposed construction*: any unused address location regardless of position

c. *Court's construction*: Plain and ordinary meaning.

The Court does not believe that Defendant has provided sufficient support to define "any available address location" as any "unused" address location, regardless of position. Defendant relies primarily on prosecution history to support its position, but it is not evident that this "clarifies the meaning of 'available'" (as Defendant argues). (D.I. 92 at p. 42). It is not self-evident to the Court that to overcome the prior art, related to spinning disks, this patent had to write data to unused spaces rather than merely available ones. *See id.* Therefore, the Court adopts Plaintiffs' construction.

5. "write operations pending" / "pending write operations" ('187 patent - claims 1, 3, 5, 7, 9, 11, 12, 14)

a. *Plaintiffs' proposed construction*: Plain and ordinary meaning

b. *Defendant's proposed construction*: write operations in buffer memory queued for the current write device(s)

c. *Court's construction*: Plain and ordinary meaning

The Court agrees with Plaintiffs that the claims do not specify where the write operations occur, whether that is in the buffer memory or elsewhere. The patent claims already reference the "current write device," so it is unnecessary to repeat this language. *See, e.g.*, '187 patent at 12:60-63 ("the controller allows write operations pending for each current write device to finish…). Therefore the plain and ordinary meaning is correct.

C. The '475 Patent

Claim 14 of the '475 patent is representative:

> A storage system for storing data used by a plurality of hosts, each host capable of transmitting *blocks of data*, the storage system comprising:
>
> a plurality of storage array devices for storing *blocks of data* transmitted by the plurality of hosts;
>
> a *channel adapter* associated with a corresponding one of the hosts, the *channel adapter* including a first data block integrity unit for *applying* and storing error detection information *associated with the transmitted blocks of data*; and
>
> a *storage array adapter* associated with a corresponding one of the storage array devices, the *storage array adapter* including a second data block integrity unit for retrieving data blocks from the corresponding storage array device and checking the error detection information associated with the stored *blocks of data*.

('475 patent, claim 14).

1. "channel adapter" ('475 patent - claims 14, 15, 17).

a. *Plaintiffs' proposed construction*: A module that sends data to or receives data from a channel

b. *Defendant's proposed construction*: front-end device interfacing between host(s) and global memory

c. *Court's construction*: A module that sends data to or receives data from a channel

A construction for "channel adapter" should not include "global memory," as Defendant asserts, because dependent claim 17 introduces the "global memory" requirement, which is not in claim 14. *See* '475 patent at 8:16-32, 8:39-40 ("The storage system of claim 14 further comprising a global memory connected between the channel adapter and storage array adapter."). It would make no sense, therefore, to read in a "global memory" requirement when the patent explicitly recites the requirement in one of the claims featuring "channel adapter," but not another. The Court also finds that there is no support for the use of "front-end device" in the construction. Therefore, the Court adopts Plaintiffs' construction.

2. "storage array adapter" ('475 patent - claims 14, 17).

a. *Plaintiffs' proposed construction*: A module that stores data in or retrieves data from a storage array device

b. *Defendant's proposed construction*: back-end device interfacing between global memory and disk or other nonvolatile storage device(s)

c. *Court's construction*: A module that stores data in or retrieves data from a storage array device

For the same reasons given for the term "channel adapter," it is not appropriate to read "global memory," or "back-end device," into this construction. Defendant also provides no support for its "nonvolatile" storage device language. *See* D.I. 92 at p. 50. Therefore, the Court adopts Plaintiffs' construction.

3. "applying" ('475 patent - claim 14).

    a. *Plaintiffs' proposed construction*: Attaching to the blocks of data.

    b. *Defendant's proposed construction*: Appending.

    c. *Court's construction*: Attaching to the blocks of data.

The Court agrees with Plaintiffs that "appending" incorrectly limits applying data to the end of something, and there is no support for such a construction. Instead, "applying" appears to encompass more broadly attaching to the blocks of data. While Defendant is correct that the patent specification describes instances of "appending" to a block of data (D.I. 92 at pp. 54-55), the use of "appending" elsewhere is not dispositive. The claims use "applying," not "appending," when the language "appending" was clearly available for use. It can reasonably be inferred that, because "appending" appears elsewhere in the patent, the choice of "applying" must be meaningful. Therefore, applying must mean attaching to the blocks of data, not merely appending to them.

4. "block(s) of data" ('475 patent - claims 1, 2, 14).

    a. *Plaintiffs' proposed construction*: Plain and ordinary meaning

    b. *Defendant's proposed construction*: fixed-size unit(s) of data

    c. *Court's construction*: Plain and ordinary meaning

Defendant argues that the patent describes hosts transmitting blocks that are a fixed size per host. (D.I. 92 at p. 56). The patent, however, describes hosts using blocks of different sizes. *See* '475 patent at 2:43-45 ("For example, one host may define a block as being 512 bytes, while another may define a block as being 520 bytes."). Defendant argues that the disclosures only refer to fixed size per host, even if they may vary from host to host. (D.I. 92 at p. 59). The patent does not foreclose different sizes per host even if it is true that it only disclosed variations from host to host. Therefore, the Court agrees with Plaintiffs that the plain and ordinary meaning should govern, and there is no limitation that a host can only provide one-size units of data.

5. "associated with the transmitted blocks of data" ('475 patent - claim 14).

a. *Plaintiffs' proposed construction*: Plain and ordinary meaning

b. *Defendant's proposed construction*: individually calculated from each of the transmitted block(s) of data

c. *Court's construction*: individually calculated from each of the transmitted block(s) of data

Defendant argues that because the invention involves computing error detection codes for individual blocks of data, such a limitation must be read into claim 14. (D.I. 92 at pp. 59-60). Plaintiffs argue that the distinction between multiple-block and individual error-detecting code is confined to claims 1 and 8 of the patent, which refer to "individual error detecting code for the block of data." ('475 patent at 7:6-7; 7:37-38). Defendant is right that the patent highlights error detecting code for individual blocks of data, distinguishing the invention from other methods that use multiple-block error detecting code. ('475 patent at 2:16-19 ("In essence, the method provides an error detecting code for individual blocks of data, rather than relying on the multiple-

block error detecting code normally provided with the plurality of blocks of data (e.g., a sector of disk)."). The specification, therefore, is clear that "associated with the transmitted blocks of data" cannot include multiple-block error detection codes. "Where the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question." *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001). The patent identifies the benefits of using error detecting code for individual blocks of data. ('475 patent at 2:21-23 ("...because an error detecting code is generated for each individual block, increased reliability in maintaining data integrity is provided.")). Claims 1 and 8 do mention "individual error detecting code," but claim 14 is independent of claims 1 and 8, describing a storage system. According to the specification, this "storage system includes data integrity units which provides error detection for individual blocks of data ... rather than relying on multiple-block error detection schemes normally provided by the hosts themselves and associated with larger blocks of data (e.g., a sector of disk)." ('475 patent at 3:58-64).

Highlighting the benefits of using error detecting code for individual blocks of data, as well as disparaging the limitations of using multiple-block error detection codes, demonstrates the patent's disavowal of the prior art. "[R]epeated derogatory statements ... reasonably may be viewed as a disavowal of that subject matter from the scope of the [p]atent's claims." *Chicago Bd. Options Exch., Inc. v. Int'l Sec. Exch., LLC*, 677 F.3d 1361, 1372 (Fed. Cir. 2012) (internal citations omitted). Therefore, this term should not cover multiple-block error detection codes, but only error detecting code for individual blocks of data. The Court consequently adopts the construction of "individually calculated from each of the transmitted block(s) of data."

D. The '556 Patent

Claim 1 of the '556 patent is representative:

> A *memory system*, comprising:
>
> a plurality of *memory boards*, each of the *memory boards* having a respective plurality of *memory segments* that may store respective data values, the segments being grouped into parity sets such that each of the parity sets includes respective segments of number N, the number N being an integer, the N respective segments in each respective parity set including a respective parity segment and N-1 respective data segments, the N respective segments in each respective parity set being distributed among the *memory boards* such that none of the *memory boards* has more than one respective segment from each respective parity set, and a respective data value stored in a respective parity segment in at least one parity set may be calculated by a logical exclusive-or of respective data values stored in respective data segments in the at least one parity set, wherein:
>
> each *memory board* includes a respective plurality of *memory regions*,
>
> each *memory region* includes a respective subset of the segments included in a respective *memory board*, and
>
> each of the segments included in a respective *memory region* may be assigned a respective base memory address different from other respective base memory addresses that may be assigned to other segments included in the respective *memory region.*

('556 patent, claim 1).

1. "memory board" ('556 patent - claims 1, 5, 6, 10, 14, 15).

    a. *Plaintiffs' proposed construction*: Plain and ordinary meaning

    b. *Defendant's proposed construction*: cache memory board(s)

    c. *Court's construction*: Plain and ordinary meaning.

Defendant argues that every embodiment of the invention in the patent is located in the "shared cache memory resource," and therefore, memory board must refer to cache memory board. (D.I. 92 at 64-67). But the patent explicitly states that although the subject invention is

described with a cache memory system, it can be used in connection with other types of memory systems:

> Although the following Detailed Description will proceed with reference being made to illustrative embodiments and methods of use of the present invention, it should be understood that it is not intended that the present invention be limited to these illustrative embodiments and methods of use. On the contrary, many alternatives, modifications, and equivalents of these illustrative embodiments and methods of use will be apparent to those skilled in the art. For example, although the subject invention will be described as being used to advantage in connection with a cache memory system in a network data storage subsystem, the subject invention may be used in connection with other types of memory systems.

('556 patent at 4:25-32).

The patent acknowledges that the use of cache memory system is but one memory system that can apply the invention. It follows then that there may be others that do not use a cache memory system. Therefore, the Court adopts Plaintiffs' construction.

2. "memory system" ('556 patent - claims 1, 2, 5-8, 10, 15).

   a. *Plaintiffs' proposed construction*: Plain and ordinary meaning.

   b. *Defendant's proposed construction*: cache memory system

   c. *Court's construction*: Plain and ordinary meaning.

For the same reasons given for the construction of "memory board," the Court construes "memory system" under its plain and ordinary meaning.

3. "memory region" ('556 patent - claims 1, 6, 10, 15).

   a. *Plaintiffs' proposed construction*: A subset of memory on a memory board that can be accessed simultaneously with other memory regions

b. *Defendant's proposed construction*: a portion of a memory board that is separately byte addressable by the cache memory system

c. *Court's construction*: A subset of memory on a memory board that can be accessed.

For reasons already explained in the construction of "memory board," the Court finds it improper to import the "cache memory" limitation. The Court also finds the difference between "subset of memory on a memory board" and "portion of memory board" to be immaterial.

The competing constructions, therefore, differ materially only with "can be accessed simultaneously" and "separately byte addressable." Defendant argues that its language of "separately byte addressable" explains that "each of the segments may have a different base memory address" to overcome prior art examined during the prosecution history. (D.I. 92 at 74). The Court agrees with Plaintiffs that the claims already address each segment having a different base memory address. *See, e.g.*, '556 patent at claim 1 ("each of the segments included in a respective memory region may be assigned a respective base memory address different from other respective base memory addresses..."). Therefore, it is unnecessary to import this limitation into the claims as Defendant has done.

Plaintiffs argue that a memory region may be simultaneously accessed because that is disclosed by a patent that was incorporated into the '556 patent, and because simultaneous access distinguished the '556 patent from prior art during the prosecution history. (D.I. 92 at pp. 70-72). Meanwhile, Defendant argues that the simultaneous access feature was not explicitly imported as a limitation to the '556 patent. (D.I. 92 at p. 73). The Court agrees with Defendant. Plaintiffs' strongest support for its position comes from an expert witness, who believes that one skilled in the art would understand the '556 patent to teach "memory region" may be

simultaneously accessed with other memory regions. (D.I. 93-2 at 104-107). The expert witness was swayed by the incorporation of the '933 patent, as well as distinguishing the '556 patent from prior art called Tuma. *Id.* The Court is not so sure. The '556 patent does incorporate by reference the '933 patent. ('566 patent at 7:26-31). But Plaintiffs have not demonstrated that the '556 patent then incorporates a simultaneous access limitation to "memory region" that comes from the '933 patent, even if the latter patent does contain such a limitation. Next, Plaintiffs and their expert infer that the '556 patent must have simultaneous access because the Tuma reference did not have it, and the '556 patent was distinguished from Tuma during prosecution. (D.I. 93-2 at 104-107). Such reasoning requires several leaps of logic. It may be the case that Tuma did not have simultaneous access. But the '556 patent could have been distinguished from the Tuma prior art in any of other number of ways—not necessarily because Tuma did or did not have simultaneous access. Nowhere do Plaintiffs demonstrate that to overcome Tuma in the prosecution history simultaneous access was explicitly adopted. Therefore, the Court cannot adopt Plaintiffs' construction. Instead, the Court's construction is, "A subset of memory on a memory board that can be accessed."

4. "memory segments" ('556 patent - claims 1, 5-7, 10, 14-16).

a. *Plaintiffs' proposed construction*: Plain and ordinary meaning

b. *Defendant's proposed construction*: a predetermined-size portion of cache memory that is separately byte addressable by the cache memory system

c. *Court's construction*: Plain and ordinary meaning

For reasons stated above, the Court is not persuaded to include "cache memory" or "separately byte addressable" language into this construction. In the briefing, scant attention is

given to the inclusion of "predetermined-size portion," and Defendant has not provided sufficient support for such a construction. Therefore, the Court will construe "memory segments" as having its plain and ordinary meaning.

IV. CONCLUSION

Within five days the parties shall submit a proposed order consistent with this Memorandum Opinion suitable for submission to the jury.